Claims 12 to 20 are active in this application of which claim 20 has been indicated to be allowable and has been rewritten in independent form.

Claims 12, 13, 15 and 16 were rejected under 35 U.S.C. 102(e) as being anticipated by Van Buskirk (U.S. 6,001,689). The rejection is respectfully traversed.

It is respectfully noted that the provisional application upon which the subject application is based and which contains the same disclosure as the subject application was filed September 30, 1997, this date being prior to the filing date of Van Buskirk which is January 16, 1998. Accordingly, Van Buskirk is not available as a reference under 35 U.S.C. 102(e) or 103(a).

Claims 18 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Van Buskirk in view of Woo (U.S. 5,926,711). The rejection is respectfully traversed for reasons stated above since Van Buskirk is not available as a reference.

Claims 14 and 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ban Buskirk in view of Chan (U.S. 6,051,467). The rejection is respectfully traversed for reasons stated above since Van Buskirk is not available as a reference.

Claim 20 was indicated to be allowable and has been rewritten in independent form so that this claim should now be allowed. A clean copy of this claim is attached hereto.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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20. An integrated circuit, comprising:

a first dielectric layer disposed outwardly from a substrate;

a plurality of gate stacks, each gate stack comprising:

a floating gate body disposed outwardly from the first dielectric layer;

a second dielectric region disposed outwardly from the floating gate body; and

a first polysilicon layer disposed outwardly from the second dielectric region;

a plurality of dielectric isolation regions disposed between the gate stacks, the dielectric isolation regions formed after the formation of the gate stacks;

a second. polysilicon layer disposed outwardly from the first polysilicon layer and the dielectric isolation regions;

a peripheral dielectric layer disposed outwardly from the second polysilicon layer and a peripheral region of the substrate, the peripheral region of the substrate disposed adjacent to a region of the substrate supporting the gate stacks;

at least one peripheral gate body disposed outwardly from the peripheral region of the substrate.